IL260/IL261/IL262

## High Speed Five-Channel Digital Isolators

## Functional Diagrams



IL262

## Features

- +5 V / +3.3 V CMOS/TTL Compatible
- High Speed: 110 Mbps
- Extended Temperature Range $\left(-40^{\circ} \mathrm{C}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$
- $2500 \mathrm{~V}_{\mathrm{RMS}}$ Isolation (1 min.)
- 2 ns Typical Pulse Width Distortion
- 100 ps Typical Pulse Jitter
- 4 ns Typical Propagation Delay Skew
- 10 ns Typical Propagation Delay
- $30 \mathrm{kV} / \mu \mathrm{s}$ Typical Common Mode Rejection
- Low EMC Footprint
- 2 ns Channel-to-Channel Skew
- 0.3" and 0.15" 16-pin SOIC Packages
- UL1577 and IEC 61010-2001 Approved


## Applications

- ADCs and DACs
- Multiplexed Data Transmission
- Data Interfaces
- Board-to-Board Communication
- Digital Noise Reduction
- Operator Interface
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting
- Plasma Displays


## Description

NVE's IL260-Series five-channel high-speed digital isolators are CMOS devices manufactured with NVE’s patented* IsoLoop ${ }^{\circledR}$ spintronic Giant Magnetoresistive (GMR) technology.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns , achieving the best specifications of any isolator. The unique fifth channel can be is used to distribute isolated clocks or handshake signals to multiple delta-sigma A/D converters. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

Typical transient immunity of $30 \mathrm{kV} / \mu \mathrm{s}$ is unsurpassed. Performance is specified over the temperature range of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ without derating.

IL260-Series Isolators are available in 0.3 " and 0.15 " 16 -pin SOIC packages. In the 0.15 " packages, the five-channel devices provide the highest channel density available.

## Absolute Maximum Ratings

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Storage Temperature | $\mathrm{T}_{\mathrm{S}}$ | -55 |  | 150 | ${ }^{\circ} \mathrm{C}$ |  |
| Ambient Operating Temperature ${ }^{(1)}$ | $\mathrm{T}_{\mathrm{A}}$ | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |  |
| Supply Voltage | $\mathrm{V}_{\mathrm{DD} 1}, \mathrm{~V}_{\mathrm{DD} 2}$ | -0.5 |  | 7 | V |  |
| Input Voltage | $\mathrm{V}_{\mathrm{I}}$ | -0.5 |  | $\mathrm{~V}_{\mathrm{DD}}+0.5$ | V |  |
| Output Voltage | $\mathrm{V}_{\mathrm{O}}$ | -0.5 |  | $\mathrm{~V}_{\mathrm{DD}}+0.5$ | V |  |
| Output Current Drive | $\mathrm{I}_{\mathrm{O}}$ | -10 |  | 10 | mA |  |
| Lead Solder Temperature |  |  |  | 260 | ${ }^{\circ} \mathrm{C}$ | 10 sec. |
| ESD |  | 2 |  | kV | HBM |  |

## Recommended Operating Conditions

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Ambient Operating Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |  |
| Supply Voltage | $\mathrm{V}_{\mathrm{DD1} 1}, \mathrm{~V}_{\mathrm{DD} 2}$ | 3.0 |  | 5.5 | V | $3.3 / 5.0 \mathrm{~V}$ Operation |
| Logic High Input Voltage | $\mathrm{V}_{\mathrm{IH}}$ | 2.4 |  | $\mathrm{~V}_{\mathrm{DD}}$ | V |  |
| Logic Low Input Voltage | $\mathrm{V}_{\mathrm{IL}}$ | 0 |  | 0.8 | V |  |
| Input Signal Rise and Fall Times | $\mathrm{t}_{\mathrm{IR}}, \mathrm{t}_{\mathrm{IF}}$ |  |  | 1 | $\mu \mathrm{~s}$ |  |

## Insulation Specifications

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Creepage Distance (external) |  | 4.03 |  |  | mm |  |
| 0.15" SOIC |  | 8.08 |  |  | mm |  |
| 0.3" SOIC |  |  | 0.2 |  | $\mu \mathrm{~A}_{\text {RMS }}$ | $240 \mathrm{~V}_{\text {RMS }}$ |
| Leakage Current ${ }^{(5)}$ |  |  | $>10^{14} \\| 7$ |  | $\Omega \\| \mathrm{pF}$ |  |
| Barrier Impedance ${ }^{(5)}$ |  |  | 5 |  | pF | $\mathrm{f}=1 \mathrm{MHz}$ |
| Capacitance (Input-Output) ${ }^{(5)}$ | $\mathrm{C}_{\mathrm{r}-0}$ |  |  |  |  |  |

## Safety and Approvals

## IEC61010-2001

TUV Certificate Numbers:
N1502812, N1502812-101

## Classification as Reinforced Insulation

| Model | Package | Pollution Degree | Material Group | Max. Working <br> Voltage |
| :--- | :---: | :---: | :---: | :---: |
| IL260, IL261, IL262 | 0.3 " 16-pin SOIC | II | III | 300 V $_{\text {RMS }}$ |
| IL260-3, IL261-3, IL262-3 | $0.15 " 16-$ pin SOIC | II | III | 150 V $_{\text {RMS }}$ |

## UL 1577

Component Recognition Program File Number: E207481
Rated 2500 V $_{\text {RMS }}$ for 1 minute (SOIC, PDIP)

## Soldering Profile

Per JEDEC J-STD-020C, MSL=2

## IL260 Pin Connections

| 1 | $\mathrm{IN}_{1}$ | Input 1 |
| :---: | :---: | :---: |
| 2 | $\mathrm{GND}_{1}$ | Ground |
| 3 | $\mathrm{IN}_{2}$ | Input 2 |
| 4 | $\mathrm{IN}_{3}$ | Input 3 |
| 5 | $\mathrm{IN}_{4}$ | Input 4 |
| 6 | $\mathrm{V}_{\text {DD1 }}$ | Supply Voltage 1 |
| 7 | $\mathrm{IN}_{5}$ | Input 5 |
| 8 | $\mathrm{GND}_{1}$ | Ground |
| 9 | $\mathrm{GND}_{2}$ | Ground |
| 10 | $\mathrm{OUT}_{5}$ | Output 5 |
| 11 | $\mathrm{OUT}_{4}$ | Output 4 |
| 12 | $\mathrm{OUT}_{3}$ | Output 3 |
| 13 | $\mathrm{OUT}_{2}$ | Output 2 |
| 14 | $\mathrm{OUT}_{1}$ | Output 1 |
| 15 | $\mathrm{GND}_{2}$ | Ground |
| 16 | $\mathbf{V}_{\text {DD2 }}$ | Supply Voltage 2 |

## IL261 Pin Connections

| $\mathbf{1}$ | $\mathbf{V}_{\mathbf{D D} 1}$ | Supply Voltage 1 |
| :---: | :---: | :--- |
| $\mathbf{2}$ | $\mathbf{G N D}_{1}$ | Ground |
| $\mathbf{3}$ | $\mathbf{I N}_{\mathbf{1}}$ | Input 1 |
| $\mathbf{4}$ | $\mathbf{I N}_{2}$ | Input 2 |
| $\mathbf{5}$ | $\mathbf{I N}_{3}$ | Input 3 |
| $\mathbf{6}$ | $\mathbf{I N}_{\mathbf{4}}$ | Input 4 |
| $\mathbf{7}$ | $\mathbf{O U T}_{5}$ | Output 5 |
| $\mathbf{8}$ | $\mathbf{G N D}_{1}$ | Ground |
| $\mathbf{9}$ | $\mathbf{G N D}_{2}$ | Ground |
| $\mathbf{1 0}$ | $\mathbf{I N}_{\mathbf{5}}$ | Input 5 |
| $\mathbf{1 1}$ | $\mathbf{O U T}_{\mathbf{4}}$ | Output 4 |
| $\mathbf{1 2}$ | $\mathbf{O U T}_{3}$ | Output 3 |
| $\mathbf{1 3}$ | $\mathbf{O U T}_{\mathbf{2}}$ | Output 2 |
| $\mathbf{1 4}$ | $\mathbf{O U T}_{\mathbf{1}}$ | Output 1 |
| $\mathbf{1 5}$ | $\mathbf{G N D}_{\mathbf{2}}$ | Ground |
| $\mathbf{1 6}$ | $\mathbf{V}_{\mathbf{D D} 2}$ | Supply Voltage 2 |

## IL262 Pin Connections

| $\mathbf{1}$ | $\mathbf{V}_{\mathbf{D D} 1}$ | Supply Voltage 1 |
| :---: | :---: | :--- |
| $\mathbf{2}$ | $\mathbf{G N D}_{\mathbf{1}}$ | Ground |
| $\mathbf{3}$ | $\mathbf{I N}_{\mathbf{1}}$ | Input 1 |
| $\mathbf{4}$ | $\mathbf{I N}_{2}$ | Input 2 |
| $\mathbf{5}$ | $\mathbf{I N}_{3}$ | Input 3 |
| $\mathbf{6}$ | $\mathbf{O U T}_{\mathbf{4}}$ | Output 4 |
| $\mathbf{7}$ | $\mathbf{O U T}_{5}$ | Output 5 |
| $\mathbf{8}$ | $\mathbf{G N D}_{1}$ | Ground |
| $\mathbf{9}$ | $\mathbf{G N D}_{\mathbf{2}}$ | Ground |
| $\mathbf{1 0}$ | $\mathbf{I N}_{\mathbf{5}}$ | Input 5 |
| $\mathbf{1 1}$ | $\mathbf{I N}_{4}$ | Input 4 |
| $\mathbf{1 2}$ | $\mathbf{O U T}_{\mathbf{3}}$ | Output 3 |
| $\mathbf{1 3}$ | $\mathbf{O U T}_{\mathbf{2}}$ | Output 2 |
| $\mathbf{1 4}$ | $\mathbf{O U T}_{\mathbf{1}}$ | Output 1 |
| $\mathbf{1 5}$ | $\mathbf{G N D}_{\mathbf{2}}$ | Ground |
| $\mathbf{1 6}$ | $\mathbf{V}_{\mathbf{D D 2}}$ | Supply Voltage 2 |



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### 3.3 Volt Electrical Specifications ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ )

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Quiescent Current IL260 <br>  IL261 <br>  IL262 | $\mathrm{I}_{\mathrm{DD} 1}$ |  | $\begin{gathered} 300 \\ 1.5 \\ 3 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 400 \\ 2 \\ 4 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |  |
| $\begin{array}{ll}\text { Output Quiescent Current } & \text { IL260 } \\ & \text { IL261 } \\ \text { IL262 }\end{array}$ | $\mathrm{I}_{\mathrm{DD} 2}$ |  | $\begin{gathered} 6.5 \\ 5 \\ 3.5 \end{gathered}$ | $\begin{gathered} 10 \\ 8 \\ 6 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
| Logic Input Current | $\mathrm{I}_{\mathrm{i}}$ | -10 |  | 10 | $\mu \mathrm{A}$ |  |
| Logic High Output Voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{DD}}-0.1$ | $\mathrm{V}_{\mathrm{DD}}$ |  | V | $\mathrm{I}_{\mathrm{O}}=-20 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}}$ |
|  |  | $0.8 \times \mathrm{V}_{\mathrm{DD}}$ | $0.9 \times \mathrm{V}_{\mathrm{DD}}$ |  |  | $\mathrm{I}_{\mathrm{O}}=-4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}}$ |
| Logic Low Output Voltage | $\mathrm{V}_{\text {OL }}$ |  | 0 | 0.1 | V | $\mathrm{I}_{\mathrm{O}}=20 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\text {IL }}$ |
|  |  |  | 0.5 | 0.8 |  | $\mathrm{I}_{\mathrm{O}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{L}}$ |
| Switching Specifications |  |  |  |  |  |  |
| Maximum Data Rate |  | 100 | 110 |  | Mbps | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Minimum Pulse Width ${ }^{(7)}$ | PW | 10 |  |  | ns | 50\% Points, $\mathrm{V}_{0}$ |
| Propagation Delay Input to Output (High to Low) | $\mathrm{t}_{\text {PHL }}$ |  | 12 | 18 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Propagation Delay Input to Output (Low to High) | $\mathrm{t}_{\text {PLH }}$ |  | 12 | 18 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Pulse Width Distortion $\left\|\mathrm{t}_{\text {PHL }}-\mathrm{t}_{\text {pLH }}\right\|^{(2)}$ | PWD |  | 2 | 3 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Propagation Delay Skew ${ }^{(3)}$ | $\mathrm{t}_{\text {PSK }}$ |  | 4 | 6 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Output Rise Time (10\%-90\%) | $\mathrm{t}_{\mathrm{R}}$ |  | 2 | 4 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Output Fall Time (10\%-90\%) | $\mathrm{t}_{\mathrm{F}}$ |  | 2 | 4 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Common Mode Transient Immunity (Output Logic High to Logic Low) ${ }^{(4)}$ | $\left\|\mathrm{CM}_{\mathrm{H}},\left\|, \mathrm{CM}_{\mathrm{L}}\right\|\right.$ | 20 | 30 |  | kV/ $\mu \mathrm{s}$ | $\mathrm{V}_{\mathrm{CN}}=300 \mathrm{~V}$ |
| Channel-to-Channel Skew |  |  | 2 | 3 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Dynamic Power Consumption ${ }^{(6)}$ |  |  | 140 | 240 | $\mu \mathrm{A} / \mathrm{MHz}$ | per channel |
|  | Magnetic Fiel | munity ${ }^{(8)}$ | D2 $=3 \mathrm{~V}, 3 \mathrm{~V}$ | ${ }_{1}<5.5 \mathrm{D}$ |  |  |
| Power Frequency Magnetic Immunity | $\mathrm{H}_{\text {PF }}$ | 1000 | 1500 |  | A/m | $50 \mathrm{~Hz} / 60 \mathrm{~Hz}$ |
| Pulse Magnetic Field Immunity | $\mathrm{H}_{\mathrm{PM}}$ | 1800 | 2000 |  | A/m | $\mathrm{t}_{\mathrm{p}}=8 \mu \mathrm{~s}$ |
| Damped Oscillatory Magnetic Field | $\mathrm{H}_{\text {OSC }}$ | 1800 | 2000 |  | A/m | $0.1 \mathrm{~Hz}-1 \mathrm{MHz}$ |
| Cross-axis Immunity Multiplier ${ }^{(9)}$ | $\mathrm{K}_{\mathrm{X}}$ |  | 2.5 |  |  |  |

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## 5 Volt Electrical Specifications ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ )

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Quiescent Current IL260 <br>  IL261 <br>  IL262 | $\mathrm{I}_{\mathrm{DD} 1}$ |  | $\begin{gathered} 350 \\ 2.5 \\ 5 \\ \hline \end{gathered}$ | $\begin{gathered} 500 \\ 3 \\ 6 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
| $\begin{array}{ll}\text { Output Quiescent Current } & \text { IL260 } \\ & \text { IL261 } \\ & \text { IL262 }\end{array}$ | $\mathrm{I}_{\mathrm{DD} 2}$ |  | $\begin{gathered} 10 \\ 7.5 \\ 5 \\ \hline \end{gathered}$ | $\begin{gathered} 15 \\ 12 \\ 9 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |  |
| Logic Input Current | $\mathrm{I}_{\mathrm{i}}$ | -10 |  | 10 | $\mu \mathrm{A}$ |  |
| Logic High Output Voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{DD}}-0.1$ | $\mathrm{V}_{\mathrm{DD}}$ |  | V | $\mathrm{I}_{\mathrm{O}}=-20 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}}$ |
|  |  | $0.8 \times \mathrm{V}_{\mathrm{DD}}$ | $0.9 \mathrm{x} \mathrm{V}_{\mathrm{DD}}$ |  |  | $\mathrm{I}_{\mathrm{O}}=-4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IH}}$ |
| Logic Low Output Voltage | $\mathrm{V}_{\text {OL }}$ |  | 0 | 0.1 | V | $\mathrm{I}_{\mathrm{O}}=20 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\text {IL }}$ |
|  |  |  | 0.5 | 0.8 |  | $\mathrm{I}_{\mathrm{O}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IL}}$ |
| Switching Specifications |  |  |  |  |  |  |
| Maximum Data Rate |  | 100 | 110 |  | Mbps | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Minimum Pulse Width ${ }^{(7)}$ | PW | 10 |  |  | ns | 50\% Points, $\mathrm{V}_{0}$ |
| Propagation Delay Input to Output (High to Low) | $\mathrm{t}_{\text {PHL }}$ |  | 10 | 15 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Propagation Delay Input to Output (Low to High) | $\mathrm{t}_{\text {PLH }}$ |  | 10 | 15 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Pulse Width Distortion $\left\|\mathrm{t}_{\text {PHL }}-\mathrm{t}_{\text {PLH }}\right\|^{(2)}$ | PWD |  | 2 | 3 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Pulse Jitter ${ }^{(10)}$ | $\mathrm{t}_{\mathrm{J}}$ |  | 100 |  | ps | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Propagation Delay Skew ${ }^{(3)}$ | $\mathrm{t}_{\text {PSK }}$ |  | 4 | 6 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Output Rise Time (10\%-90\%) | $\mathrm{t}_{\mathrm{R}}$ |  | 1 | 3 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Output Fall Time (10\%-90\%) | $\mathrm{t}_{\mathrm{F}}$ |  | 1 | 3 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Common Mode Transient Immunity (Output Logic High to Logic Low) ${ }^{(4)}$ | $\mid \mathrm{CM}_{\mathrm{H}}$, , $\mathrm{CM}_{\mathrm{L}} \mid$ | 20 | 30 |  | kV/ $/ \mathrm{s}$ | $\mathrm{V}_{\text {CN }}=300 \mathrm{~V}$ |
| Channel-to-Channel Skew |  |  | 2 | 3 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| Dynamic Power Consumption ${ }^{(6)}$ |  |  | 200 | 340 | $\mu \mathrm{A} / \mathrm{MHz}$ | per channel |
|  | Magnetic Fiel | munity ${ }^{(8)}$ | $\mathrm{D}_{2}=5 \mathrm{~V}, 3 \mathrm{~V}$ | $1<5.5 \mathrm{~V}$ |  |  |
| Power Frequency Magnetic Immunity | $\mathrm{H}_{\text {PF }}$ | 2800 | 3500 |  | A/m | $50 \mathrm{~Hz} / 60 \mathrm{~Hz}$ |
| Pulse Magnetic Field Immunity | $\mathrm{H}_{\mathrm{PM}}$ | 4000 | 4500 |  | A/m | $\mathrm{t}_{\mathrm{p}}=8 \mu \mathrm{~s}$ |
| Damped Oscillatory Magnetic Field | $\mathrm{H}_{\text {OSC }}$ | 4000 | 4500 |  | A/m | $0.1 \mathrm{~Hz}-1 \mathrm{MHz}$ |
| Cross-axis Immunity Multiplier ${ }^{(9)}$ | $\mathrm{K}_{\mathrm{X}}$ |  | 2.5 |  |  |  |

## Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $\left|\mathrm{t}_{\text {PHL }}-\mathrm{t}_{\text {PLH }}\right|$. \%PWD is equal to PWD divided by pulse width.
3. $\mathrm{t}_{\text {PSK }}$ is the magnitude of the worst-case difference in $\mathrm{t}_{\text {PHL }}$ and/or $\mathrm{t}_{\text {PLH }}$ between devices at $25^{\circ} \mathrm{C}$.
4. $\quad \mathrm{CM}_{\mathrm{H}}$ is the maximum common mode voltage slew rate that can be sustained while maintaining $\mathrm{V}_{\mathrm{O}}>0.8 \mathrm{~V}_{\mathrm{DD} 2}$. $\mathrm{CM}_{\mathrm{L}}$ is the maximum common mode input voltage that can be sustained while maintaining $\mathrm{V}_{\mathrm{O}}<0.8 \mathrm{~V}$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1-8 shorted and pins 9-16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 6).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0 s ; 800 ps transition time.

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## Application Information

## Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1
Residential, Commercial \& Light Industrial
Methods EN55022, EN55014
EN50082-2: Industrial Environment
Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic
Field), EN61000-4-10 (Damped Oscillatory Magnetic Field) ENV50204
Radiated Field from Digital Telephones (Immunity Test)
Immunity to external magnetic fields is even higher if the field

direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:

## Cross-axis Field Direction

## Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

## Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both $\mathrm{GND}_{1}$ and $\mathrm{GND}_{2}$ are highly recommended for data rates above 10 Mbps .
Capacitors must be located as close as possible to the $V_{D D}$ pins.

## Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

## Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$
\mathrm{PWD} \%=\frac{\text { Maximum Pulse Width Distortion (ns) }}{\text { Signal Pulse Width (ns) }} \times 100 \%
$$

For example, with data rates of 12.5 Mbps :
PWD\% $=\frac{3 \mathrm{~ns}}{80 \mathrm{~ns}} \times 100 \%=3.75 \%$
This figure is almost three times better than any available optocoupler with the same temperature range, and two times better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10\% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the $10 \%$ limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worstcase channel-to-channel skew in IL260-Series Isolators is only 3 ns , which is ten times better than any optocoupler. IL260-Series Isolators have a maximum propagation delay skew of 6 ns , which is five times better than any optocoupler.

IL260/IL261/IL262

## Application Diagram-Multi-Channel Delta-Sigma A/D Converter

In a typical single-channel delta-sigma ADC , the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:


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## Package Drawings, Dimensions and Specifications

### 0.15" 16-pin SOIC Package



## 0.3" 16-pin SOIC Package



Ordering Information and Valid Part Numbers


## Revision History

ISB-DS-001-IL260/1/2-J December 2009

ISB-DS-001-IL260/1/2-I

ISB-DS-001-IL260/1/2-H

ISB-DS-001-IL260/1/2-G

ISB-DS-001-IL260/1/2-F

ISB-DS-001-IL260/1-E

ISB-DS-001-IL260/1-D

ISB-DS-001-IL260/1-C

## Change

- Relaxed Vdd1 quiescent current specification to $500 \mu \mathrm{~A}$.

Change

- Added typical jitter specification at 5V.

Change

- Added EMC details.


## Change

- Added magnetic field immunity and electromagnetic compatibility specifications.

Change

- Added IL262 configuration
- Added note on package drawings that pin-spacing tolerances are nonaccumulating.
- Changed ordering information to reflect that devices are fully RoHS compliant with no exemptions.

Change

- Eliminated soldering profile chart

Change

- Revised application drawing
- Revised package drawings
- Misc. syntax changes

Change
Page 2: UL File Number and TUV Certificate Numbers added
Page 9: Soldering Profile added.

## IL260/IL261/IL262

## About NVE

## An ISO 9001 Certified Company

NVE Corporation is a high technology components manufacturer having the unique capability to combine spintronic Giant Magnetoresistive (GMR) materials with integrated circuits to make high performance electronic components. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometer), Digital Magnetic Field Sensors, Digital Signal Isolators and Isolated Bus Transceivers.

NVE is a leader in GMR research and in 1994 introduced the world's first products using GMR material, a line of GMR magnetic field sensors that can be used for position, magnetic media, wheel speed and current sensing.

NVE is located in Eden Prairie, Minnesota, a suburb of Minneapolis. Please visit our Web site at www.nve.com or call (952) 829-9217 for information on products, sales or distribution.

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